USB 3.0 Testing

Mike Engbretson, Chief Technology Engineer, GRL
Agenda

- GRL Involvement in USB 3.0
- USB 3.0 Technology Timeline
- USB 3.0 PHY CTS 0.9 Overview
- USB 3.0 Vendor Solutions
- Hands-On Lab Preview
GRL Involvement in USB 3.0

- Mike E. Involved in Specification and CTS development thru 2009.
  - Joined GRL January, 2010
- GRL USB-IF plugfest participation
- Seeking official USB ITL status
  - Endorsed by many USB-IF members
- GRL fully equipped and currently offering services for USB2.0 and USB3.0 pre-compliance testing
USB 3.0 Technology Timeline

<table>
<thead>
<tr>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
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<tr>
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<td></td>
<td>Test Vendor Compliance Group Participation</td>
<td>PIL (Peripheral Interop Lab)</td>
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<tr>
<td></td>
<td>April 09 0.5 Test Spec (CWG Kickoff)</td>
<td>Sept 09 0.9 Spec</td>
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<td>USB-IF Plugfests</td>
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<td></td>
<td></td>
<td></td>
<td>‘200 products have passed SuperSpeed USB certification testing’ – USB-IF, March 1, 2011</td>
</tr>
</tbody>
</table>

Today

Certified Labs

Spec Development

Silicon Phase

- Spec Development
- Product Development
- USB-IF Tool Development

Integration Phase

Deployment Phase
### Superspeed Compliance Test Requirements

#### ‘Deep Dive’

<table>
<thead>
<tr>
<th></th>
<th><strong>USB 3.0 Product Test Matrix</strong></th>
<th><strong>USB 2.0 LS/FS/HS Test Matrix</strong></th>
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<tbody>
<tr>
<td></td>
<td>USBCV Chapter 9 Tests</td>
<td>USBCV Device Specific Tests</td>
</tr>
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<td>xHCI Host Tests</td>
<td>xHCI HSET</td>
</tr>
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<td>Silicon</td>
<td>USB 3.0 Electrical</td>
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<td>End Product</td>
<td>USB 3.0 Gold Tree Interop</td>
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<td></td>
<td></td>
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<tr>
<td></td>
<td>Device</td>
<td>All 2.0 Speeds</td>
</tr>
<tr>
<td></td>
<td>Hub</td>
<td>All 2.0 Speeds</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>Hub</td>
<td>All 2.0 Speeds</td>
</tr>
<tr>
<td></td>
<td>Mass Storage Device</td>
<td>All 2.0 Speeds</td>
</tr>
</tbody>
</table>

- **Table Notes:**
  - ‘n/a’ indicates not applicable.
  - ‘All 2.0 Speeds’ indicates tests for all 2.0 speeds.
  - ‘Hub Tests’ indicates tests specific to hubs.
  - ‘MSD Tests’ indicates tests specific to mass storage devices.
USB 3.0 PHY CTS 0.9RC
Nov. 11th, 2009

- LFPS Testing
- Transmitter Compliance Test
- Receiver Compliance Test
- Found at:

LFPS Testing

- **TD1.1 – Low Frequency Periodic Signaling Test TX Test**
  - Verifies LFPS Timing Requirements
    - Trigger on first LFPS from DUT
    - Measure LFPS Parameters
      - $t_{burst}$, $t_{RiseFall2080}$, Duty Cycle,
      - $V_{CM-AC-LFPS}$, $V_{TX-DIFF-PP-LFPS}$

- **TD1.2 – Low Frequency Periodic Signaling Test RX Test**
  - Verifies DUT Recognizes LFPS
    - Signaling with voltage swings and duty cycles at specification limits
  - Device passes if DUT recognizes LFPS and starts sending TXEQ signal.
Transmitter Compliance Test Method

- Transmitter Eye Specified at TP1
- Probed at TP0
- SW Channel
  - CTLE convolved with Channel

6.7.2 Transmitter Eye
The eye mask is measured using the compliance data pattern CD1 described in Section 6.4.4. Eye Height is measured from 10^-6 UI. Jitter is extrapolated from 10^-6 UI to 10^-12.

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<th>Nominal</th>
<th>Maximum</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>100</td>
<td>1200</td>
<td>mV</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Cj</td>
<td>93</td>
<td>ps</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rj</td>
<td>60</td>
<td>ps</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tj</td>
<td>132</td>
<td>ps</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Measured over 10^-6 UI and extrapolated to 10^-12 BER
2. Measured after receiver equalization function
3. Measured at end of reference channel and cables at TP1 figure 6-14

Compliance Measured At Far End of Channel (TP1)

Figure 6-4. Channel Models without Cable (Top) and with Cable (Bottom)

CTLE

Figure 6-11. Generic Eye Mask

Figure 6-17. Tx Compliance Rx EQ Transfer Function

Figure 6-14. Tx Normative Setup with Reference Channel
Compliance Channels are defined to test Transmitter for worst case conditions.

- **Worst Case Channel for Hosts**
  - 5” Device PCB Trace
  - 3M Cable

- **Worst Case Channel for Devices**
  - 11” Device PCB Trace
  - 3M Cable
The TP0 Probing Challenge

- **Host Probing**
  - Direct Probing
  - or DeEmbed

- **Device Probing**
  - A-Connector Direct
  - B-Connector
    - DeEmbed Required

- **Short Cable + USB-IF Fixture** Adds ~2.5dB Loss at 2.5GHz Fundamental.
  - More if you wiggle it.

- Errors associated with DeEmbed
Transmitter Compliance Testing

- **TD1.3 Transmitter Eye Test**
  - Test verifies transmitter meets eye width Deterministic Jitter (Dj), and Random Jitter (Rj) with -3.5dB equalization with Reference CTLE and JTF.
  - Dj and Eye Diagram with CP0 (Scrambled0)
  - PING.Toggle used to toggle test pattern
  - Rj determined with CP1 (D10.2)
  - Apply Worst case Channel (through SW)
  - Apply SW CTLE
  - Measurements made over 1 Million UI
  - $T_j = 14 \times R_j \text{ (CP1)} + D_j \text{ (CP0)}$, per Dual-Dirac Model at $10^{-12}$ BER

Table 6.7. Compliance Pattern Sequences

<table>
<thead>
<tr>
<th>Compliance Pattern</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP0</td>
<td>D0.0 scrambled</td>
<td>A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7); however, it does not include SRP sequences.</td>
</tr>
<tr>
<td>CP1</td>
<td>D10.2</td>
<td>Nyquist frequency</td>
</tr>
<tr>
<td>CP2</td>
<td>D14.3</td>
<td>Nyquist+2</td>
</tr>
<tr>
<td>CP3</td>
<td>K28.5</td>
<td>CCM pattern</td>
</tr>
<tr>
<td>CP4</td>
<td>LPR5</td>
<td>The low frequency periodic signaling pattern</td>
</tr>
<tr>
<td>CP5</td>
<td>K28.7</td>
<td>/With de-emphasis</td>
</tr>
<tr>
<td>CP6</td>
<td>K28.7</td>
<td>/Without de-emphasis</td>
</tr>
<tr>
<td>CP7</td>
<td>50-250 1/s and 0/s</td>
<td>/With de-emphasis</td>
</tr>
<tr>
<td>CP8</td>
<td>50-250 1/s and 0/s</td>
<td>/Without de-emphasis; Repeating 50-250 1/s and then 50-250 0/s.</td>
</tr>
</tbody>
</table>

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.
Transmitter Compliance Testing

- **TD1.4 Transmitted SSC Profile Test**
  - Test verifies transmitter meets SSC profile requirements when measured at the compliance test port with -3.5dB of transmitter equalization and processed after the JTF.
  - Note: PCI Express Host Adapter is tested in a system with its own SSC profile.
  - Connect Device
  - Power Device
  - Send PING.LFPS to toggle to CP1
  - Capture 1 Million Unit Intervals
  - Measure Slew Rate $T_{CDR, SLEW_MAX}$
  - Measure $t_{SSC-MOD-RATE}$ and $t_{SSC-FREQ-DEVIAITION}$
Tx Compliance Test Considerations

- Test Vendors provide
  - Fixtures for Probing (Rogers Material)
  - Signal Processing
    - Fixture DeEmbed
    - SW Channel Convolution of 3M Cable & ‘Far End’ Channel
  - Automated Compliance Software
    - Integration of USB-IF SigTest Algorithms in automation tools

- USB-IF Provides
  - Fixtures for Probing (FR4 Material)
  - SigTest SW
    - Application of CTLE
    - Jitter & Eye Measurements
Receiver Compliance Test

- **TD1.5 - Receiver Jitter Tolerance Test**
  - Test verifies receiver properly functions in the presence of random and deterministic jitter at multiple frequencies.

**Jitter Tolerance Curve**

**Additional Requirements**
- Loopback
- 5000 PPM SSC

**Jitter Requirements**
- Periodic (sinusoidal) jitter frequencies
  - 500 KHZ – 50 MHz

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>Tolerance corner</td>
<td>4.9</td>
<td>MHz</td>
</tr>
<tr>
<td>Jj</td>
<td>Random Jitter</td>
<td>0.0121</td>
<td>UI rms</td>
</tr>
<tr>
<td>Jj_pp</td>
<td>Random Jitter peak-peak at $10^{12}$</td>
<td>0.17</td>
<td>UI p-p</td>
</tr>
<tr>
<td>Jj_sine</td>
<td>Sinusoidal Jitter</td>
<td>2</td>
<td>UI p-p</td>
</tr>
<tr>
<td>Jj_sine</td>
<td>Sinusoidal Jitter</td>
<td>1</td>
<td>UI p-p</td>
</tr>
<tr>
<td>Jj_sine</td>
<td>Sinusoidal Jitter</td>
<td>0.5</td>
<td>UI p-p</td>
</tr>
<tr>
<td>Jj_sine</td>
<td>Sinusoidal Jitter</td>
<td>0.2</td>
<td>UI p-p</td>
</tr>
<tr>
<td>Jj_sine</td>
<td>Sinusoidal Jitter</td>
<td>0.2</td>
<td>UI p-p</td>
</tr>
<tr>
<td>V_full_swing</td>
<td>Transition bit differential voltage swing</td>
<td>0.75</td>
<td>V p-p</td>
</tr>
<tr>
<td>V_EQ_level</td>
<td>Non transition bit voltage (equalization)</td>
<td>-3</td>
<td>dB</td>
</tr>
</tbody>
</table>
Rx Compliance Channels

- Compliance Channels HW Channels to test Receiver for worst case conditions

- Worst Case Channel for Hosts

- Worst Case Channel for Devices
Test Vendor Solutions

- Transmitter
- Receiver
- Interconnect
- Link Layer Test
- Protocol Analysis
USB 3.0 SuperSpeed Physical Layer Test solutions
Infiniium 90000 X-Series Oscilloscope for USB 3.0 SuperSpeed Transmitter Testing

- The Highest True Analog Bandwidth
- The Highest Measurement Accuracy
- Full 30 GHz Probing System
- The Most Comprehensive Application Specific Software

U7243A USB 3.0 TX Test Application sw
N4903B USB 3.0 SuperSpeed Receiver Testing

• Accurate and Repeatable RX Testing
• Flexible Calibration and Test Automation
• Accepted by the USBIF and Test Labs
Agilent USB 2.0 and USB 3.0 Total Solution

**PHYSICAL LAYER**

### Transmitter Characterization
- **DSAX93204A oscilloscope**

### Receiver Jitter Tolerance Testing
- **N4903B High-performance JBERT with SER Counter**
- **N4916B De-emphasis Converter**
- **N5990A Automation Software**

### Cable/Connector
- **E5071C Network Analyzer**
- **N4433A Ecal Module**
- **USB 3.0 Cab/conn test fixture kit from BitifEye**

### Test Fixtures
- **U7242A USB 3.0 Fixture**

**New**
- **U7243A USB 3.0 and N5416A USB 2.0**
- **N8805A USB 3.0 Protocol viewer software**

- **Industry's lowest scope noise floor/sensitivity and trigger jitter**
- **Automated compliance software accurate, efficient, and consistent**
- **Industries fastest and highest accuracy cable and connector test**

**Fixtures for LS, FS, HS and SuperSpeed USB Physical Layer testing**
Additional references and links

- [http://www.testroniclabs.com/](http://www.testroniclabs.com/)
- [http://www.agilent.com/find/USB](http://www.agilent.com/find/USB)
  [www.agilent.com/USB 3.0 Cable Connector Testing MOI](http://www.agilent.com/USB 3.0 Cable Connector Testing MOI)
Simplifying Validation and Debug of USB 3.0 Designs
- Tektronix USB3.0 PHY Layer Testing Solutions
Complete USB 3.0 Transmitter Solution
DPO/DSA70000B Series Oscilloscopes

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures
- Automation software for characterization and compliance
  - TekExpress with option USB-TX (includes option USB3)
- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)

TF-USB3-AB-KIT
Accurate Transmitter Characterization

Channel De-Embedding

- Measurements defined at the pins often require de-embedding of the channel to measure the true TX output
  - Characterize channel with TDR or Simulator to create S-parameters
  - Import S-Parameter file to SDLA
  - Create fixture de-embed filter with SDLA software
- Identify root cause failures
  - Removes fixture effects
  - Improved margin
Transmitter Compliance Testing (Normative Testing)

Channel Embedding

- Test methodology outlined in the USB 3.0 Compliance Test Specification
  - Currently .9 draft available on USB-IF website
- Measurements are defined at TP1
- Signal is Acquired at TP2
  - SW Channel is embedded by the Oscilloscope
  - CTLE is then applied and measurements are taken

6.7.2 Transmitter Eye

The eye mask is measured using the compliance data pattern CD1 described in Section 6.4.4. Eye Height is measured from $10^6$ UI. Jitter is extrapolated from $10^6$ UI to $10^{13}$.

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<td>1200</td>
<td></td>
<td>mV</td>
<td>2</td>
</tr>
<tr>
<td>$D_j$</td>
<td>93</td>
<td>ps</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_j$</td>
<td>60</td>
<td>ps</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_j$</td>
<td>132</td>
<td>ps</td>
<td>1,2,3</td>
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Notes:
1. Measured over $10^6$ UI and extrapolated to $10^{13}$ BER
2. Measured after receiver equalization function
3. Measured at end of reference channel and cables at TP1 figure 6-14

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Figure 6-14. Tx Normative Setup with Reference Channel
Custom Equalization Analysis

Create Silicon Specific CTLE Functions

- Tektronix USB Solutions ships with the USB Specification defined CTLE Function
- Customizing CTLE functions and creating filters for use with Tektronix’ USB Solution is easily achieved with SDLA (Serial Data Link Analysis Software)

\[ H(s) = \frac{A_{dc} \omega_1 \omega_2}{\omega_z} \frac{s + \omega_z}{(s + \omega_1)(s + \omega_2)} \]

\[ A_{dc} = 0.667 \]
\[ \omega_z = 2\pi \left( \frac{650 \times 10^6}{\text{Rate} \text{ (Gb/s)}} \right) \]
\[ \omega_1 = 2\pi \left( \frac{1.95 \times 10^9}{\text{Rate} \text{ (Gb/s)}} \right) \]
\[ \omega_2 = 2\pi \left( \frac{5 \times 10^9}{\text{Rate} \text{ (Gb/s)}} \right) \]
BERTScope Solution for USB 3.0 Receiver Test

1. Stressed Pattern Generation
   - Random Jitter (RJ)
   - Sinusoidal Jitter (SJ)
   - Spread Spectrum Clocking (SSC)
   - Pre-emphasis
   - Programmable for easy debug/characterization

2. Loopback initiation capability
   - Automation software performs single click loopback initiation

3. Jitter Tolerance Testing
   - Seamlessly handles clock compensation characters (SKPs for USB and PCIe and ALIGNs for SATA and SAS) for accurate BER measurement
   - Compliance test and Search modes to find device’s pass/fail point

4. Automation software
   - Further automation of receiver testing
   - Report generation
   - Easy recall and management of past tests
USB 3.0 Receiver Test Configuration

- **Automation Software**
- **Error Detector**
- **Stressed Pattern Generator**
- **Device Under Test (DUT)**

- DPP provides pre-emphasis to emulate compliant transmitter
- CR recovers a clock from the retransmitted data from the DUT
- From Stressed Pattern Generator
- To Error Detector
- Loopback
Channel and Cable Testing

*DSA8200 Sampling Oscilloscope with IConnect®*

- **Test Fixtures**
  - A Receptacle
  - B Receptacle
  - USB2/USB3 Connectors Available for Crosstalk measurements

- **Using Sampling Oscilloscope & S-Parameter SW**

- **Measurements:**
  - Impedance
  - Intra-Pair Skew
  - Differential Insertion Loss
  - Differential Return Loss
  - Differential Near-End Crosstalk
  - Differential Crosstalk between USB3.0 and USB2.0 Pairs
  - Differential to CM Conversion
Resources and events

- Tektronix USB Electrical PHY Tools
  - [www.tektronix.com/usb](http://www.tektronix.com/usb)

- USB3.0 “Meet the Experts” Session in
  - Tektronix Santa Clara Office Learning Center on April 28th
Comprehensive SuperSpeed USB Test Suite

The Right Tool for Every Stage of USB 3.0 Development

March 15, 2011
Transmitter Test

- **8 Zi and LabMaster Oscilloscopes**
  - 4Ghz to 45Ghz Bandwidths with up to 20 Channels

- **QPHY-USB3-TX**
  - Compliance Test Software provides full reporting capability including Pass/Fail indications and screenshots from pertinent tests

- **SIGTEST**
  - Electrical test software is fully integrated into the oscilloscope application

- **Eye Doctor™ II**
  - Advanced Signal Integrity Tools enables channel emulation, de-embed, and equalization which aids in debugging SuperSpeed USB compliance failures

- **SDA II**
  - Allows fast eye diagram creation and jitter analysis on long memory acquisitions

- **USB3bus D and ProtoSync**
  - USB3.0 symbol and packet decode for debugging
Receiver Test

- **PeRT3 Test System**
  - Protocol-enabled Receiver and Transmitter Tolerance Tester provides a new level of intelligent capability for receiver testing
  - Capable of interpreting and generate protocol traffic, the PeRT3 is uniquely able to manage link training for fully-automated testing
  - Fully programmable internal jitter and noise sources for tolerance and compliance testing

- **QPHY-USB3-RX**
  - Compliance Test Software provides full reporting capability including Pass/Fail indications and screenshots from pertinent tests

- **Calibrating the Jitter Output of the PeRT3**
  - Receiver test specifications require calibration of the jitter output sources for the test instrument. When using the PeRT3 in conjunction with SDA 8 Zi oscilloscope, this calibration is done automatically by the QPHY-USB3-Tx-Rx application
  - Manual jitter calibration is also available
Automated Test Solutions

- **QualiPHY Automated Test Engine**
  - Fully integrates and automates transmitter and receiver testing. QPHY-USB3-Tx-Rx permits the scope to communicate directly with the PeRT3 and RF switch automating all instruments and creating compliance reports that include both transmitter and receiver results.

- **QPHY-USB3-Tx-Rx**
  - Supports all transmitter compliance tests as described by the SuperSpeed USB Electrical Compliance Test Specification and selected tests in accordance with the Universal Serial Bus 3.0 Specification
Cable and Return Loss Testing

- **TDR/T-based S-parameter Test Set for Signal Integrity**
  - 40 GHz frequency range on up to 4 ports
  - Built-in automatic OSLT calibration
  - Single button press operation
  - Fraction of the cost of a VNA
  - Fast calibration and measurement time
  - Small footprint (12” x 12” x 6”) and Portable (17 lbs)

- **Signal Integrity Tools You Expect**
  - Differential & common-mode step response at input and output ports
  - Mixed-mode return loss to 40 GHz
  - TDR traces shown during measurement
  - Differential & common-mode insertion loss to 40 GHz
  - Mode conversion step responses
  - Differential & common-mode impedance vs. electrical length
  - Rise time normalization for all time domain results
  - Up to 16 measurements can be displayed simultaneously
USB 3.0 Link Layer Compliance

- What is Tested?
  - Link and Packet Robustness
  - CRC Error handling
  - Invalid Link Commands
  - Timer Deadlines
  - LGOOD / LCRD Sequences
  - U0/U1/U2/U3 under controlled conditions
  - Link Reset
    - Detection and Initiation
LeCroy USB 3.0 Compliance Suite

Automated Test Console for Link, Physical, Framework Layers & Device Class
**TD.7.02 Link Command Framing**

- PUT must recognize LCs with only 3 out of 4 valid SLC symbols

PUT fails if:
- If link enters LC timeout
- LC Packets not successfully received
- link doesn’t stay U0 for at least 50 ms.
When LGOOD_x is delayed, PUT must observe 3µs Header ACK time-out before starting Recovery.

The test fails if:

- link doesn’t wait 3 µs for LGOOD handshake
- link doesn’t stay U0 for at least 50 ms.
The test fails unless:

- PUT Sends 16 TS2 w/Reset bit asserted
- PUT Sends at least 2 TS2 with Reset bit de-asserted
- PUT Sends at least 16 idles
- PUT Transitions to U0
- PUT must transmit correct Header Seq and Credit Advertisement
- PUT must NOT send Port Capability LMP
SuperSpeed USB 3.0
Protocol Analyzer, Traffic Emulator for Hosts and Devices, and Compliance Tester

Ellisys USB Explorer 280
World’s First Protocol Test Solution for SuperSpeed USB 3.0
Examiner™ Compliance Test Suite

Device Test Setup

Examiner automatically executes selected tests, optionally through an EX280 Analyzer, to the device under test.

Host Test Setup

Examiner automatically executes selected tests, optionally through an EX280 Analyzer, to the host under test.

Coverage:

- Chapter 6 (Physical Layer)*
- Chapter 7 (Link Layer)*
- Chapter 9 (Device Framework)
- Electrical Tests for U0, U1, U2, U3 and VBus
- Mass Storage

*Will soon be required for certification.

Test Go/No-Go decisions are made in hardware (not software). Result: precise characterizations and fast testing (about 45-90 seconds)!

Easy, Automated GUI for Test Suite Selection
USB BusXpert

- Based on SerialTek’s highly successful SAS/SATA GUI
  - Time synced correlation of SAS/SATA and USB into one trace
- Strong focus on storage related protocols (UAS, BULK, etc)
  - Decode capability unmatched in the industry for ease of use
- Largest buffers available, 18GB, 9GB, 4.5GB or 2GB
- Most powerful analyzer on the market
- Flexible licensing options to fit all budgets/performance needs
Interactive Real-time USB 3.0 Analysis with Total Phase
# Top Beagle USB 5000 Benefits

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefits</th>
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<tr>
<td><strong>Interactive Real-Time</strong></td>
<td>• Only solution with true real-time display</td>
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<td><strong>Instant Class-Level Decoding</strong></td>
<td>• Automatic decode and display of most popular USB classes</td>
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<td><strong>Advanced Triggering</strong></td>
<td>• Flexible state-based advanced triggering</td>
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<td><strong>Fast</strong></td>
<td>• Fastest capture and upload time</td>
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<td>• Search and filter during capture</td>
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<td><strong>Multi-platform support</strong></td>
<td>• Industry’s only solution supporting Windows®, Linux and Mac OS</td>
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Hands-On Lab Preview

- **Schedule**
  - **9-10am** - USB 3.0 CTS 0.9 Overview and Introduction to Vendor Test Tools
  - **10:15a-12noon** - Hands-On Lab #1
  - **1200 – 1:00p**  Catered Lunch
  - **1pm-3pm**  Hands-On Lab #2
  - **3:15p-5pm**  Hands-On Lab #3
Hands-On Lab Preview

- **Lab 1 - Physical Layer Transmitter Testing**
  - Transmitter Compliance Testing – Learn to perform a USB 3.0 Transmitter ‘Plug Fest’ Compliance Test
  - Determining your Transmitters True Margin – Learn to De-Embed test fixture and cable losses from your measurements

- **Lab 2 - Receiver Physical Layer Testing**
  - Receiver Compliance Testing – Learn to perform a USB 3.0 Receiver ‘Plug Fest’ Compliance Test
  - Receiver Margin Testing – Learn how to determine how much margin you have in your Receiver design

- **Lab 3 - Cable S-Parameter Creation:**
  - S-Parameter Measurement – Learn to measure Cable and Fixture losses
  - Understanding TouchStone Files – Learn the structure of industry standard file format for S-parameters
Thank You For Attending

- Brought to you by Granite River Labs...
  Your Bay Area USB Test Lab

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